In the claims:

Please amend the claims as follows:

1.(Currently Amended): A method for designing a logic circuit comprising:

selecting and placing graphical library elements of the logic circuit using a graphical user interface;

maintaining a data structure representative of a model, the model including combinational blocks, state elements and graphical library elements of the logic circuit; and

generating an architectural model and an implementation model from the data structure.

2.(Original): The method of claim 1 wherein the data structure comprises a description of a net list.

3.(Original): The method of claim 2 wherein the data structure comprises:

elements representing logical functions;

elements representing connection points to gates;

elements representing all bits of a simulation state; and

elements representing an arbitrary collection of bits within the simulation state.

4.(Currently amended): The method of claim ~~4~~ 3 wherein the elements are all C++ classes.

5.(Original): The method of claim 1 wherein the architectural model comprises C++ software code.

6.(Original): The method of claim 1 wherein the implementation model comprises Hardware Design Language (HDL).

7.(Original): The method of claim 6 wherein the HDL is Verilog.

8.(Original): The method of claim 6 wherein the HDL is Very high speed integrated circuit Hardware Design Language (VHDL).

9.(Currently Amended): A method comprising:

specifying a model containing combinatorial blocks, state elements and graphical library elements using a graphical user interface;

maintaining a descriptive net list of the model; and

generating a C++ model and a Verilog model from the descriptive net list.

10.(Canceled)

Cntd A2

11.(Original): The method of claim 9 wherein the net list comprises gates, nodes and nets.

12.(Original): The method of claim 9 wherein maintaining comprises parsing and analyzing the combinatorial blocks, state elements and graphical library elements of the model.

13.(Original): The method of claim 9 wherein generating comprises:

partitioning a topology of the net list into a plurality of partitions; and

code ordering each of the partitions.

14.(Currently Amended): A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

specify a model containing combinatorial blocks, state elements and graphical library elements using a graphical user interface;

maintain a descriptive net list of the model; and

generate a C++ model and a Verilog model from the descriptive net list.

15.(Original): The computer product of claim 14 wherein the computer readable medium is a random access memory (RAM).

16.(Original): The computer product of claim 14 wherein the computer readable medium is a read only memory (ROM).

17.(Original): The computer product of claim 14 wherein the computer readable medium is a hard disk drive.

18.(Currently Amended): A processor and memory configured to:

specify a model containing combinatorial blocks, state elements and graphical library elements using a graphical user interface;

maintain a descriptive net list of the model; and

generate a C++ model and a Verilog model from the descriptive net list.

Canted A2

19.(Original): The processor and memory of claim 18 wherein the processor and memory are incorporated into a personal computer.

20.(Original): The processor and memory of claim 18 wherein the processor and memory are incorporated into a network server residing in the Internet.

21.(Original): The processor and memory of claim 18 wherein the processor and memory are incorporated into a single board computer.

22.(Original): A system comprising:

a graphic user interface (GUI) for receiving parameters from a user to generate a model and displaying the model, the model containing combinatorial blocks, state elements and graphical library elements;

a maintenance process to manage a data structure representing a descriptive net list of the model; and

a code generation process to generate a C++ model and a Verilog model from the data structure.

23.(Original): The system of claim 22 wherein the data structure comprises gates, nodes and nets.

24.(Original): The system of claim 22 wherein the maintenance process comprises parsing and analyzing the combinatorial blocks, state elements and graphical library elements of the model.

Cont'd A2

25.(Original): The system of claim 22 wherein the code generation process comprises:

partitioning a topology of the net list into a plurality of partitions; and

code ordering each of the partitions.

26 - 28.(Withdrawn)